AMENDMENTS TO THE SPECIFICATION

Please amend paragraph number 44 as follows.

[0044] Voltage divider 105 of Fig. 2 is coupled to linearizer circuit 120 of feedback loop 37. Linearizer circuit 120 receives the divided analog voltage signal ~~70~~ 70' at its input 120a from node 117 of voltage divider 105. Linearizer circuit 120 is utilized in a case where the particular power detector 65 used (see, e.g., Fig. 4) outputs a non-linear voltage signal 70, as depicted by the graph on the right side of Fig. 2, but the downstream bias circuit 40 (see, e.g., Fig. 6) is linear. Linearizer 120 linearizes analog voltage signal ~~70~~ 70', and outputs a linearized analog voltage signal ~~70~~ 70'' that is approximately linear as a function of power, as depicted by the voltage signal ~~70~~ 70'' graph on the left side of Fig. 2.

Please amend paragraph number 46 as follows.

[0046] The linearizer 120 is coupled to bias circuit 40, and provides the divided, linearized analog voltage signal ~~70~~ 70'' from its output 120b to bias circuit 40. Bias circuit 40 is coupled to a bias connection point of first amplifier stage 125 of amplifier 35. As discussed below, bias circuit 40 uses the linearized analog voltage signal 70 to control an amount of a variable quiescent current 45 that first amplification stage 125 of amplifier 35 draws from a fixed-level DC voltage source Vcc, thereby optimizing the current consumption of amplifier 35 for a selected linearity given the output power level previously selected by baseband processor 10 for the RF signal 30 output by amplifier 35.

Please amend paragraph number 62 as follows.

[0062] Figure 5 is a schematic diagram of an embodiment of a linearizer circuit 300 that may be used as linearizer 120 of Fig. 1. Linearizer circuit 300 receives the divided analog voltage signal ~~70~~ 70' (Figs. 1, 2) at its input 301 from node 117 of voltage divider 105 (Fig. 2), and provides a voltage signal 70'' at its output 328 that varies proportionally with analog voltage signal 70 and is approximately linear as a function of the output power of the amplifier. ~~True?~~ In this embodiment, linearizer circuit 300 includes a differential amplifier built around NPN transistors 312 and 320.

Please amend paragraph number 65 as follows.

[0065] In operation, voltage signal ~~70~~ 70' passes to the base of transistor 312 via resistor 302 and node 304. The differential amplifier formed by transistors 312 and 320 amplifies a difference between the voltages at the bases of transistors 312 and 320. The DC bias at the base of transistor 320 is fixed, and the voltage at the base of transistor 312 is compared to this voltage. If, for the sake of example, analog voltage signal ~~70~~ 70' was zero, all current in the differential amplifier would pass through transistor 320, resulting in a relatively large voltage drop across resistor 318 and a relatively low base level voltage at output 328. As the voltage at the base of transistor 312 passes the voltage at the base of transistor 320 due to the voltage of analog voltage signal ~~30~~ 70, the current in the differential amplifier is shifted from transistor 320 to transistor 312. This reduces the current I_1 through resistor 318, and thus increases the voltage of the voltage signal at output 328 beyond the base level mentioned

above. As mentioned, the voltage signal 70'' at output 328 varies proportionally with the voltage of analog voltage signal 70 and ~~is~~ can be made to be an approximately linear function of the power of RF signal 30 through proper choice of the resistors 314, 316, and 321.

Please amend paragraph number 67 as follows.

[0067] Figure 6 is a schematic diagram of an exemplary bias circuit 400, which may be used as bias circuit 40 of Fig. 1. Input 442 of bias circuit 400 is coupled to receive the linearized voltage signal 70'' provided at output 328 of linearizer circuit 300 of Fig. 5. Input 442 is coupled to the base of an NPN transistor 446 of bias circuit 400. The collector of NPN transistor 446 is coupled to the fixed-level DC voltage source Vcc. A resistor 450 is coupled between the emitter of transistor 446 and a node 456. Transistor 446 is in an emitter follower configuration. Resistor 454 is coupled between voltage source Vcc and node 456.

Please amend paragraph number 71 as follows.

[0071] In operation, the bias circuit 400 of Figure 6 receives the linearized analog voltage signal 70'' provided at output 328 of linearizer circuit 300. The resulting voltage at node 442 causes transistor 446 to pass a current from Vcc through resistor 450. The current through resistor 450 continuously varies in proportion to the continuously-varying voltage of voltage signal 70. A fixed-level current also is drawn from voltage source Vcc through resistor 454. The current through resistors 450 and 454 flows through transistor 460 via node 456.